

**R09**

**Code No: 09A70412**

**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD**

**B. Tech IV Year I Semester Examinations, May/June - 2013**

**VLSI Design**

**(Common to ECE, EIE, BME, IT, ETM, ECM, ICE)**

**Time: 3 Hours**

**Max. Marks: 75**

**Answer any Five Questions  
All Questions Carry Equal Marks**

---

- 1.a) Explain the fabrication process of p-well CMOS transistor with neat diagrams.
- b) Explain about ion implantation mechanism for fabrication of ICs. [9+6]
- 2.a) Find the drain-to-source current versus voltage relationship of  $I_{ds}$  vs  $V_{ds}$  of nMOS transistor.
- b) Explain about latch-up effect in CMOS transistor. [9+6]
- 3.a) Draw the stick diagram of CMOS two input NAND gate.
- b) Explain about various contact cuts are used for CMOS transistor design and fabrication. [7+8]
- 4.a) Implement two input EX-NOR gate by using transmission gates.
- b) Explain about pseudo-nMOS logic with an example? Compare the performance of pseudo nMOS logic with nMOS logic? [7+8]
- 5.a) Explain the operation of 4X4 Barrel Shifter with its circuit diagram.
- b) Design a 4 bit Comparator which gives outputs  $A=B$ ,  $A>B$  and  $A<B$ . [8+7]
- 6.a) Explain the operation of DRAM Cell.
- b) Explain about Serial access memories. [8+7]
- 7.a) Implement the following functions by using PLA.  
 $F1(a,b,c) = \sum m(1,2,4,7)$   
 $F2(a,b,c) = \sum m(1,2,3,7)$
- b) Draw and explain the architecture of FPGA? [7+8]
- 8.a) Explain the stuck at fault models with suitable examples.
- b) Explain how an improved layout can be reduced faults in CMOS circuits. [8+7]

--ooOoo--