

**R09**

**Code No: 09A30503**

**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY, HYDERABAD**

**B.Tech II Year I Semester Examinations, May/June-2013**

**Digital Logic Design**

**(Computer Science and Engineering)**

**Time: 3 hours**

**Max. Marks: 75**

**Answer any five questions  
All questions carry equal marks**

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- 1.a) Convert the Decimal Number **35.45** into corresponding Octal Number.  
b) Using 2's complement method perform. [7+8]  
 $(68)_{10} - (42)_{10}$
- 2.a) Explain any four basic theorems of Boolean algebra with necessary proofs.  
b) Explain the truth tables of universal logic gates. [8+7]
3. Reduce the following function using K-map technique and implement using NAND Gates.  
 $F(A, B, C, D) = \sum m(1, 3, 7, 11, 15) + d(0, 2, 5)$  [15]
- 4.a) Explain the basic operation of  $4 \times 1$  Multiplexer.  
b) Implement the following function using  $8 \times 1$  Multiplexer  
 $F(A, B, C, D) = \sum m(1, 3, 5, 6, 7)$  [5+10]
- 5.a) Explain the basic difference between Combinational and Sequential circuits.  
b) Explain the basic operation of JK Master Slave Flip-Flop with truth tables. [5+10]
- 6.a) Draw and explain the 4 bit Shift Register with necessary example.  
b) Explain the basic principles of Ripple counter. [8+7]
- 7.a) Compare PROM, PLA and PAL.  
b) Implement the following functions using PLA  
 $A(X, Y, Z) = \sum m(1, 2, 4, 6)$   
 $B(X, Y, Z) = \sum m(0, 1, 6, 7)$  [5+10]
8. Explain the concept of Hazards in combinational logic circuits with some design example. [15]

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